

[illegible]

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Group Art Unit: Unknown

Examiner: Unknown

For: HIGH FREQUENCY LOW COST PACKAGE FOR SEMICONDUCTOR DEVICES

Commissioner for Patents
Washington, D.C. 20231

Prior to examination, please amend the above-identified application as follows:

Amend the specification by inserting before the first line the sentence:

IN THE CLAIMS:

Please cancel claims 2-22 without prejudice or disclaimer.

Please add the following new claims:

Claims 23-43 are added as new claims.

23. A method of making an interconnectable package comprising:

providing a first wafer having a plurality of bottom die;
providing a second wafer having a plurality of top die;
patterning at least one transmission line on at least one side of said bottom die of said first wafer;
etching at least one integral connector and at least one transmission line on said top die of said second wafer;
coupling a component to each of said plurality of bottom die of said first wafer;
forming a wafer stack by bonding said second wafer to said first wafer such that said top die of said second wafer is aligned with said bottom die of said first wafer; and
dicing said wafer stack into a plurality of individual packets wherein each of said plurality of packets contains a top die having said integral connector bonded to said bottom die having a component.

24. The method of making an interconnectable package of claim 23, further comprising: etching an aperture in said top die of said second wafer such that said component may be placed through said aperture and coupled to said bottom die of said second wafer after the bonding and dicing of said first and second wafer.

25. The method of making an interconnectable package of claim 23 wherein a cap is bonded over said aperture after said component is placed through said aperture.

26. The method of making an interconnectable package of claim 23, wherein the component is an integrated circuit.

27. The method of making an interconnectable package of claim 26, wherein the integrated circuit is an millimeter microwave integrated circuit.

28. The method of making an interconnectable package of claim 23, wherein the component is an optical fiber.

29. The method of making an interconnectable package of claim 23, wherein the component is an optical semiconductor.

30. The method of making an interconnectable package of claim 23, wherein the integral connector etched on said top die of said second wafer is shaped as a male connection component.

31. The method of making an interconnectable package of claim 23, wherein the integral connected etched on said top die of said second wafer is shaped as a female connection component.

32. The method of making an interconnectable package of claim 23, wherein the integral connected etched on said top die of said second wafer is shaped as a hermaphrodite connection component.

33. The method of making an interconnectable package of claim 23, wherein the integral connected etched on said top die of said second wafer is shaped as a female connection component.

34. A method of making a dielectric package for housing a component and having an integral connection member comprising:

providing a first die having at least one conductor patterned on the die;

providing a second die having at least one conductor patterned on said second die;

bonding said second die to said first die such that the conductor on said first die is aligned with said conductor on said second die.

35. The method of making a dielectric package for housing a component and having an integral connection member of claim 34, wherein the first die is formed having a female shape.

36. The method of making a dielectric package for housing a component and having an integral connection member of claim 34, wherein the second die is formed having a male shape.

37. The method of making as dielectric package for housing a component and having an integral connection member of claim 36, further comprising:

coupling a component to said first die prior to bonding the second die to said first die.

38. The method of making as dielectric package for housing a component and having an integral connection member of claim 34, further comprising:

etching an aperture into said second die.

39. The method of making as dielectric package for housing a component and having an integral connection member of claim 38, wherein a component is placed through said aperture on said second die and coupled to said first die after the second die is bonded to the first die.

40. The method of making as dielectric package for housing a component and having an integral connection member of claim 34, wherein the component is an integrated circuit.

41. The method of making a dielectric package for housing a component and having an integral connection member of claim 40, wherein the integrated circuit is a millimeter microwave integrated circuit.

42. The method of making a dielectric package for housing a component and having an integral connection member of claim 34, wherein the component is an optical fiber.

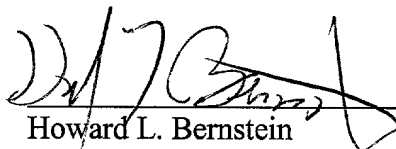
43. The method of making a dielectric package for housing a component and having an integral connection member of claim 34, wherein the component is an optical semiconductor.

Preliminary Amendment
U.S. Appln. No. Unknown

REMARKS

Entry and consideration of this Amendment is respectfully requested.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "H. Bernstein", written over a horizontal line.

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